Standard Instrument Controller

System Design Review

Meeting Report

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Revision Date: 22 April 1994
Revision Number: 9
Approved By:

1 INTRODUCTION

This document is the report of the System Design Review for the Gemini Standard Instrument Controller workpackage, which took place at RGO Cambridge on 11–12 April, 1994. The review was attended by:

- R.J. McGonegal, Gemini Controls Manager
- P.M. McGehee, Gemini Real Time Engineer
- J. Oschmann, Gemini Systems Engineer
- J.M. Stewart, UK Gemini Work Package Manager
- A.N. Johnson, Work Package Responsible for the SIC

The body of report has been derived from a document presented at the review by the WPR, which included various pertinent details, described the progress of the workpackage development and raised various questions for discussion. A list of items for further action has been placed at the end of this report, in preference to spreading these throughout the body of the text.

2 SIC HARDWARE

2.1 Agreed Hardware List

The hardware to be purchased for the SIC consists of one or more of each of the items listed below (see section below for quantities).

2.1.1 Workstation

- Sun SPARCstation Classic, 32Mb RAM, 535Mb Internal HDD, 20" Colour display
- 1Gb External HDD pack
- Ethernet Transceiver

2.1.2 VMEbus Crate

- Heurikon MSE/12 Rack, 12 VMEbus slots, 110/240V PSU, Cooling fans

2.1.3 IOC

- Motorola MVME167-33, MC68040, 33MHz, 16Mb RAM, Ethernet, 4 RS232
- Motorola MVME712M Transition Module for I/O Connections
- Ethernet Transceiver

2.1.4 Time Bus

- Bancomm bc635VME, disciplined oscillator, IRIG-B I/O
- Bancomm bc637VME, GPS Satellite Receiver, disciplined oscillator, IRIG-B I/O

2.1.5 Synchro Bus

- VMIVME-5578, 256KB Reflective Memory, Fibre-Optic Interface, 26Mbyte/sec
- Fibre-Optic Cable

2.1.6 Motor Controllers

- DeltaTau PMAC-VME/4, DSP56001, Programmable, Control up to 4 DC Servos
- Oregon Microsystems VME-8 Stepper Controller

2.1.7 I/O Cards

- XYCOM XVME240, 80 channel TTL I/O
- XYCOM XVME566, 32 channel, 12 bit Analogue Input
- VMIC VMIVME4100, 16 channel, 12 bit Analogue Output

2.2 Prices

The UK prices below are the prices which the project should have to pay, assuming that the information about the payment of import duty and VAT are accurate. For items sourced in the UK, the price includes VAT. Items which are to be purchased from the UK distributor of a US manufacturer are assumed to be exempt from import duty and VAT as they will be returned to the USA after the end of the workpackage.

2.2.1 Delivery Timescales

Items	Delivery
UK Supplier	

SPARC Classic	< 6 weeks
Sun Microsystems	
Heurikon MSE/12	?
(USA)Diamond Point	
Motorola MVME167	~ 4 weeks
Crellon Microsystems	
Bancomm bc635VME	6 weeks
Dean Microsystems	
Bancomm bc637VME	6 weeks
Dean Microsystems	
VMIC VMIVME-5578	8 weeks
Dean Microsystems	
DeltaTau PMAC-VME/4	4 weeks
Naples Coombe Ltd	
XYCOM XVME240	4 weeks
Dean Microsystems	
XYCOM XVME566	4 weeks
Dean Microsystems	
VMIC VMIVME-4100	8 weeks
Dean Microsystems	

3 HARDWARE INSTALLATION

3.1 Approach To Installation

The following approach will be used to check out and install the SIC hardware.

- For each item below, make notes during the installation process for use later when writing the installation documentation.

3.1.1 VMEbus Crate

- Read documentation
- Visual Inspection
- Cabling
- Jumper settings
- Tests — backplane voltages, fans etc.

3.1.2 MVME167

- Read manual
- Visual inspect
- Set jumpers
- MVME712M installation
- Card installation
- Connections to MVME712M
- Tests — using MVMEbug diagnostics

3.1.3 Other VME Cards

- Read manual
- Visual inspection
- Set jumpers
- Card installation and external connections
- Tests — read/write registers using MVMEBug

3.2 Documentation Coverage

The hardware installation documentation to be produced as part of the work package will include the following information:

- Fnal hardware list, including addresses, UK suppliers & prices
- Description of installation steps to be performed
- Overview of manufacturers' documentation
- Reference documentation for the hardware installation, including differences from default settings (note for MV167 about MVMEBug vs. VxWorks Prom settings)
- Some "What to do if..." steps, or a fault tree

4 SOFTWARE INSTALLATION

4.1 Approach To Installation

The activities to be performed under the title of Software Installation specifically exclude setting up the Solaris Operating System, which is a specialised task and is assumed to be performed by a trained systems administrator. However the Installation Planning activity below may produce some information which will be needed by the sysadmin during the Operating System set-up.

The work will involve two phases.

- Installation Planning (disk structure, ownership, permissions etc.)
- Package Installation. For each of the packages below, make notes while following the manufacturers instructions for use when writing the installation documentation.

4.1.1 VxWorks

- Install software on host
- Install MV167 Proms
- Set jumpers
- Test VxWorks installation

4.1.2 EPICS

- Install software on host
- Build host & target binaries
- Boot MV167 & IOCCore
- Build & run test database, possibly using the SSC Test Stand example

4.2 Documentation Coverage

The software installation documentation to be produced as part of the work package will include the following information:

- Notes for system administrators on Solaris & disk installation, user set-up & permissions etc.
- Software list, disk size, brief overview of license conditions
- Standard Installation Documentation
- Description of installation steps/differences to standard
- Resulting installation structure, as planned (including disk tree)

5 TIME BUS

5.1 Environmental Model

See Appendix A.

5.2 Hardware Needed

The minimum hardware required to develop the Time Bus software varies with the different phases of the development. For the majority of the time, the following will be sufficient:

- Host Workstation (Sun Classic)
- 1 IOC (VME Chassis and MVME167 CPU card)
- Time card (Bancomm bc635VME and/or bc637VME)

For some debugging and testing stages, including acceptance testing, the hardware required will be:

- Host Workstation
- 2 IOCs
- Both Time cards, installed in separate IOCs

5.3 Time Bus Package Requirement Specification

The following are extracts from the Time Bus PRS, which is available separately. They summarise the specific functional and performance requirements of the software, and the additional work which will be required before the software specifications can be completed.

5.3.1 Functional Requirements

5.3.1.1 Database Timestamp Maintenance

EPICS maintains a Timestamp for every database record which stores the time when it was last processed. For an IOC which has a Bancomm card installed, the value to be placed in the timestamp should be read from the card.

5.3.1.2 Current UTC

A database programmer will be able to define an EPICS database record which provides the current value of UTC as an accessible field. The field will return the time in the standard EPICS timestamp format.

5.3.1.3 Periodic Interrupts

The driver and device layers will support a programmable periodic I/O interrupt from the Bancomm hardware which can be used to initiate database processing and EPICS Event generation within the IOC.

5.3.1.4 Specific Time Interrupt

A “one-shot” interrupt facility similar to the periodic interrupt will be supported, which can be used to initiate database processing at a time given in a field of a time record.

5.3.1.5 External Event UTC

An TTL signal may be connected to the Bancomm card and used to signal the occurrence of an external event. When the event is signal occurs, the value of UTC will be latched by the card and an interrupt be generated. Driver and device layer support is required so that a suitably initialised database record will cause the event to generate an EPICS I/O Interrupt thus initiating record processing and permitting the latched time to be read. The record processing provides the ability to generate an EPICS event as a direct result of the I/O Interrupt.

5.3.1.6 Hardware Status Reporting

The EPICS alarm reporting system will be used to indicate error status conditions from the Bancomm hardware. Errors reported will include the loss of an incoming time reference signal (GPS or IRIG-B as appropriate).

5.3.2 Anticipated Time Bus Trade/Design Studies

5.3.2.1 Use Of UTC Vs. TAI

UTC causes problems associated with the occasional addition of leap seconds. Since UTC is synchronised from GPS, the hardware will automatically apply leap second correction. The same correction must be made by the Telescope Control System at the identical moment if the sky position is to remain correct. Alternatives to this necessary synchronism would be to use Atomic Time TAI, which is never corrected by the addition of leap seconds, or some other similar time standard. A trade study is proposed to look at alternative local time standards to UTC. Some external input will be needed from the Observatory Control System and/or Telescope Control System developers on this issue.

5.3.2.2 NTP Support

Bancomm sell a complete GPS Network Time Server system which provides a source of IRIG-B time codes and also functions as a Stratum One NTP time server over TCP/IP. It should be possible to use this system in place of the bc637VME card, and a trade study will evaluate this proposal for advantages and problems which this would give. In the event of this being rejected, alternative means of providing a Stratum One NTP server to the Gemini systems using the GPS cards in an IOC will be examined.

5.3.2.3 VxWorks Support

It may be desirable to provide time support to VxWorks using the Bancomm hardware, including possibly generating the VxWorks system clock interrupt this way. The advantages and disadvantages of this will be the subject of a trade study, which will also consider whether to provide a C-callable interface to obtain the current time and control other facilities on the cards.

5.3.2.4 Record Types

The datatype of an EPICS Timestamp consists of a pair of 32-bit Integers, holding nanoseconds and seconds since 1st January 1990. EPICS does not currently provide a means of accessing or manipulating timestamps from within an EPICS database, thus some consideration is needed as to what type of record the Time Bus interface should support. There may be some call to provide a string record, but a numeric datatype will be essential for some applications which need to manipulate the time. This trade study will also consider the creation of a new record type to access and manipulate timestamps.

5.3.3 Performance Requirements

No specific performance requirements have been identified yet. The aim is to produce an efficient interface with minimal time delay being introduced by the driver and device software.

6 SYNCHRO BUS (REFLECTIVE MEMORY)

6.1 Environmental Model

See Appendix A.

6.2 Hardware Needed

Varies during development. For the initial work, the following will be sufficient:

- Host Workstation (Sun Classic)
- IOC (VME Chassis and MVME167 CPU card)
- Reflective Memory card (VMIVME-5578)

For the later development, debugging and testing stages, including acceptance testing, the hardware required will be:

- Host Workstation
- 2 IOCs
- Both Reflective Memory cards in separate IOCs

6.3 Synchro Bus Package Requirement Specification

The following are extracts from the Synchro Bus PRS, which is available separately. They summarise the specific functional and performance requirements of the software, and the additional work which will be required before the software specifications can be completed.

6.3.1 Functional Requirements

6.3.1.1 Output Records

A database programmer will be able to declare an EPICS analogue, long, string or waveform output record with a reflective memory address. A value written into the VAL field of such a record will be broadcast to all reflective memory input records declared in other IOCs which have the same reflective memory address.

6.3.1.2 Input Records

An input record declared within the reflective memory will report the value of the field at the time of record processing. Record types to be supported are as for the output record above.

6.3.1.3 Status Reporting

The VMIC Reflective Memory hardware provides a means to test the integrity of the fibre-optic cable under software control. The device driver will perform periodic tests of the ring state, and report this to the higher level EPICS software using the standard EPICS Alarm State/Severity mechanism.

6.3.2 Anticipated Synchro Bus Trade/Design Studies

6.3.2.1 C Subroutine Interface

The ability to interface directly to the Reflective Memory from a C subroutine may be a useful requirement. This trade study will examine the VMIC programming model and propose a suitable interface specification for a VxWorks driver. Note that this same subroutine interface should be used between the EPICS device and driver layers, but may not utilise all the features provided for C subroutines.

6.3.2.2 Use Of Interrupts

The VMIC cardset provides the ability to send 3 different types of interrupt between memory nodes, either broadcast or to a specific node number. A trade study will examine the different ways in which this functionality could be used, including estimates of the effect of broadcast interrupts on the performance of an IOC.

6.3.2.3 Reflective Memory Allocation

An EPICS record which is connected to the Reflective Memory must be associated with an address in the memory space. There are several possible ways in which this memory space can be partitioned and allocated to the different records and nodes, and these will be presented within a trade study. This study will also examine and recommend a method by which records can be protected from being written to by more than one IOC, which would result in the loss of data.

6.3.3 Performance Requirements

6.3.3.1 Array Data Transmission Delay

A series of 10 32-bit floating point numbers representing Zernike polynomial coefficients shall be able to be transmitted between two IOCs at an update rate of 200Hz, with a maximum delay of TBD microseconds from source to destination records.

6.4 Existing Driver

A driver already exists at Argonne for the VMIVME-5578 card, but this only supports Analogue I/O record types. It is hoped that this record can be used as a basis for the further development required by Gemini, but it is possible that significant changes may have to be made to it.

7 DELTATAU PMAC

7.1 Environmental Model

See Appendix A.

7.2 Hardware Needed

The following items should be sufficient to develop and debug the software.

- Host Workstation (Sun Classic)
- IOC (VME Chassis and MVME167 CPU card)
- DeltaTau card (PMAC-VME/4)

The availability of the following items during software development would slightly increase confidence in the software. These items are available in Tucson and may be brought over to the UK on loan for acceptance testing:

- Power-Amplifier
- DC Motor
- Encoder

7.3 Delta Tau Driver Package Requirement Specification

The following are extracts from the DeltaTau PMAC PRS, which is available separately. They summarise the specific functional and performance requirements of the software, and the additional work which will be required before the software specifications can be completed.

7.3.1 Functional Requirements

7.3.1.1 PMAC Command Interface From Vxworks

A C subroutine interface will be provided which will enable a VxWorks program to send command messages to the PMAC card and retrieve any response returned by the command.

7.3.1.2 PMAC Command Interface From Epics

An EPICS record type will be developed which will support the control of a PMAC card from an EPICS database. This will permit all PMAC commands to be sent and any responses read back. Command strings can be sent individually via a command string field, or by providing the name of a disk file which contains a series of commands to be sent all at once. The latter permits fairly complex settings to be sent to the card in a single database process cycle, including the sending of motion program

7.3.2 Anticipated PMAC Trade/Design Studies

7.3.2.1 C Subroutine Interface

The facilities to be provided by the C subroutine interface need to be examined in more detail — a non-blocking interface might increase the complexity of the driver software, but could save development work in higher level software. This trade study will examine the PMAC programming model and propose a suitable interface specification for the VxWorks driver. Note that this same subroutine interface should be used between the EPICS device and driver layers, but may not utilise all the features provided for C subroutines.

7.3.3 Performance Requirements

No specific performance requirements have been identified yet. The aim is to produce an efficient interface with little delay between the arrival of a command string and its transmission to the PMAC card or before its response is reported to the higher level software.

8 STEPPER MOTOR RECORD MODIFICATIONS

A Package Requirements Specification for this work will be developed in the next workpackage phase and presented at the Preliminary Design Review. The descriptions below summarise the work which needs to be done.

8.1 Reasons For Modification

All standard EPICS database record types provide a means of using the record without connecting it directly up to some supporting hardware, either by providing Simulation fields, or by supporting a Soft Record type. This makes it relatively easy for a database designer to create a system which will operate as a simulator, without being connected up to the hardware it is designed to control.

The existing Stepper Motor Record type as released with EPICS includes neither Simulation nor Soft Record support, thus a database which controls stepper motors using this record type will only run properly in an IOC which is connected to the hardware it is meant to drive. The ability to simulate absent hardware is a standard requirement for Gemini software. While it is probably possible to create a database which includes a wrapper around the Stepper Motor record so it is not used when in simulation mode, it is obviously preferable that the record type should support simulation directly.

8.2 Additions Proposed

It is proposed that software simulation be added to the Stepper Motor Record type, and that the modified type be offered back to the EPICS consortium for inclusion in a later release of EPICS. Returning the modified software to the consortium will ensure that future releases of EPICS will include derivatives of the new driver and thus still provide simulation support.

8.3 Anticipated Trade/Design Studies

8.3.1 Simulation Fields Or Soft Record

It is thought likely that the additions will be in the form of Simulation fields, but this decision will form a Trade study which will look at the two options.

8.4 Discussion

A question was raised regarding the standards to be followed and documentation required for this development — should we improve the documentation of the existing stepper motor record, which is not particularly well described at present? The current project plan assumes that there will not be a major amount of work in the area of documentation. This discussion was not conclusively resolved at the review.

9 ALLEN-BRADLEY

9.1 Allen-Bradley In The Enclosure Control System

Both the rotating and fixed portions of the ECS are likely to use Allen-Bradley PLCs in their control systems and will present a serial interface to the Enclosure Control System VME (PLC 1771-KG Serial ECS). The PLC is thought to use a reasonably standard interface protocol over this type of serial link, and it is likely that there may be a need for a record type which supports this protocol, although it ought to be possible to implement the protocol in a database by using String records for the RS232 communication. However this record would only be required for the ECS workpackage, thus any driver development which is to be done will be funded as a subcontract to that workpackage.

9.2 Allen-Bradley Remote Serial I/O

From some work done by John Maclean on the Primary Mirror Support workpackage and other comments it had become clear that the Allen-Bradley 1771 series is not a good standard for a Remote I/O bus for Gemini Control systems because of the age of the standard and the power dissipation of the bus modules. As the Interlock System (described below) will similarly not require the Allen-Bradley remote I/O that was originally envisaged in the WPD, there is now no need for the 6008-SV I/O scanner.

10 GEMINI INTERLOCK SYSTEM

10.1 Description From WPD

Sections 4.2.3.5 and 4.3.8 of the WPD describe a requirement for a derivative of the APS Personnel Safety System. The APS system provides an interface to EPICS, but the capability of this interface is limited to monitoring the state of the various interlocks. All the interlock logic in the APS-PSS is handled by Allen-Bradley PLC-5 processors.

10.2 Actual Gemini Requirements

There appear to be two fundamental requirements for the Gemini Interlock System. In both cases, the software is required to fail safe, preventing activities from occurring if the current state of the interlock cannot be read or is ambiguous.

10.2.1 Hardware Interlock Monitor

This reports the current state of a hardware interlock to the control system software. This is just a status report, there is no means of influencing the state of the interlock.

10.2.2 Interlock Interface To EPICS

This requirement provides a means for software to request that some hardware interlock be set and thus prevent some activity from occurring which might be dangerous. The software must be able to read the status of the interlock, and the information returned may include other data such as the reason for the interlock being set and what the current request state is from the software.

10.3 Interlock System Trade Study

A trade study will be performed to specify the Gemini requirements, and to indicate how the Interlock System should be implemented in EPICS. The actual implementation task including any Interlock hardware forms part of the Mount Control System workpackage.

11 EVENT BUS

A new requirement was introduced at the review, to do a brief study on how to pass TTL Event signals between an IR camera at Cassegrain and the chopping secondary at the top end with very low jitter on the signal edges. Discussion of this requirement concluded that the simplest method of doing this would be to have an optical fibre run between the two locations and purchase or develop a TTL to Fibre converter module. The requirement and this proposed solution will be written up as a short report.

12 SAMPLE CONTROL SYSTEM

The Sample Control System is an EPICS database which provides a demonstration of the all the SIC hardware and the new device drivers. It will also be used as the basis for performance measurements of the new software and supporting hardware.

12.1 Requirement From WPD

Section 5 of the WPD gives a fairly detailed description of what the Sample Control System should do, giving the Environmental and Behavioural models. It is not appropriate to develop these in greater detail until after completion of the later stages of the other software development work.

12.2 Development Plan

The project plan for the Sample Control System thus postpones any further work until the Critical Design phase. The relationship between the workpackage phases and the SCS work is given in the table below:

Workpackage Phase	**Proposed SCS Activity**
Critical Design	SCS Requirements Specification
Implementation #1	Design SCS
Implementation #2	Implement SCS
Acceptance Testing	Specify and perform Acceptance tests

13 PROJECT MANAGEMENT

13.1 Work Breakdown Structure

See the Gantt chart in Appendix B.

13.2 Project Schedule

The WBS is based on a fairly detailed model of the project plan, which has better estimates of the work required than those which were used in the earlier stages of the project. Unfortunately these estimates indicate that more work is needed than was originally allowed for. Most of this work appears in the later stages of the workpackage, and using the current plan this will result in completion around April 1995 rather than the February date given for the Acceptance Test Review. The manpower required for the project has increased in line with the extra work in the schedule.

Some discussion occurred over the estimate from Bob Dalesio at Los Alamos that it only takes a week to write a new device driver for EPICS. As an experienced EPICS developer Bob's estimate may me more accurate than the WPR, so there may be some leeway to reducing the work required at a later stage. In particular because of the simplicity of the software to be developed, there may be no advantage in reviewing the internal structure of the device driver software once the interface specification has been written. By not reviewing this stage it may be possible to do all the work required using manpower figures which are more like the original estimate. If this is done, the later stages of the project can be replanned and may have an alternate review structure.

13.3 Dates Of Future Reviews

A decision on the revised development model will be taken at PDR, the work for which would be required for either model and can be achieved by the original date. The original review dates are given in the table below.

Workpackage Review		Date
Preliminary Design Review	28 Jun. 1994	
Critical Design Review		20 Sep. 1994
Implementation Progress Review #1	24 Oct. 1994	
Implementation Progress Review #2	11 Nov. 1994	
Acceptance Test Review		20 Feb. 199

13.4 Budget

The budget for the workpackage is split into manpower for the software development activities, and the hardware costs which are given in section above. The total budget for the project is fixed; see the WPD or Work Scope for the relevant sums. With the increased manpower requirement, according to the current project plan the workpackage will go over-budget, although this will change if the development model is revised.

14 FINAL DISCUSSION

14.1 Action List

The following action items were agreed. The section numbers refer to the relevant subsection above from which the item was derived.

1. PMM /
   Check MVME712M Mounting in MSE/12
2. PMM
   Check what PMAC accessories available in Tucson
3. ANJ
   Check width of Analogue I/O cards
4. PMM
   Provide US hardware supplier information to ANJ for inclusion in hardware installation documentation
5. ANJ/SW
   Discuss standard disk layouts, user and group set-ups
6. PMM
   Check release date for EPICS R3.12
7. ANJ
   Supply SSC Test stand documentation to PMM
8. ANJ
   Check VxWorks archive for a test suite
9. RJM
   Use of periodic interrupts
10. RJM
    Backup IRIG-B Receiver or hot spare GPS
11. RJM
    Need for 1Hz, 100Hz & 1khz signals
12. PMM
    Look at WFS to Secondary Actuator Delay breakdown, supply ANJ with figure attributable to the Synchro Bus requirement
13. PMM
    PMAC Performance requirement
14. ANJ
    Show Stepper Motor Record Reference manual section to HMS for comments
15. PMM
    Command structure for ECS Interface to the PLC-5 systems
16. ANJ
    Investigate status of EPICS String support of VxWorks Serial ports
17. RJM
    Expand enclosure SDD section for ANJ
18. RJM
    ECS: Trade study for command translation
19. ANJ
    Write intro. about EPICS interface to serial line for ECS WPR
20. ANJ
    Write specification for event bus system, 2 or 3 state over Fibre
21. PMM
    User Characteristics for EPICS developers
22. ANJ
    ...ability attributes from SRS
23. RJM/PMM
    New Work Scope

24. ANJ
    Check for old Email questions to PMM not answered satisfactorily
25. ANJ/PMM
    List of goals for RJM visit in May