Appendix O

Detector Options for the LGS WFS

Summary

Six different possibilities were considered in detail for the laser guide star (LGS) wavefront sensor (WFS) camera. These are summarized in Table 1. Of the six possibilities considered, two (ADAPT3 and CCD50) were found to be incapable of meeting the design requirements, and one of these two (ADAPT3) is not being produced anymore.

Table 1: Summary of LGS WFS options

	PixelVision ADAPT3	Marconi CCD39	Marconi CCD50	Marconi CCD60	MIT/LL 64^2	MIT/LL 128^2
CCD						
format	80x80 40 output	80x80 4 output	128x128 16 output	128x128 1 output	64x64 4 output	128x128 16 output
pixel size (μm)	36	24	24	24	21 or 24	21
Detector head						
mass (kg)	9.1	0.5	0.5	?	?	?
volume (mm)	300x200x200	58x85x50	58x85x50	225x118x 77	200x340x 190	200x340x 190
number required	5	5	1	1	5	1
heat transfer	liquid	liquid	liquid	?	forced air	forced air
CCD controller						
type	integrated	ARC/SDSU2	ARC/SDSU2	integrated	integrated	integrated
host interface	fibre to PCI	fibre to PMC	fibre to PMC	parallel	RS422 to VME/ PMC	RS422 to VME/ PMC
maximum separation from head (m)	N/A	1-2	1-2	N/A	3	3
mass (kg)	N/A	17	17	N/A	?	?
volume (mm)	N/A	350x190x280	350x190x 280	N/A	310x180x 312	310x180x 330
heat transfer	liquid	liquid	liquid	?	forced air	forced air
Power supply						
mass (kg)	N/A	7.2	7.2	?	?	?
volume (mm)	N/A	135x300x210	135x300x 210	?	440x185x 335	440x185x 335
power dissipation (W)	225	240	200	?	84	67
Performance						
SNR	10.3	15.1	system too slow	12.0	15.1	15.0
Cost (USD)	no longer produced	$142000	$60700 + CCD	not yet available	$275000	$204000

Two optical configurations were included, one with 5 separate CCDs for each of the WFS positions, and one in which all 5 Shack-Hartman arrays were combined onto a single 128x128 pixel CCD. We deem the former to be preferable because of the simplified and more flexible optical design. It also has the advantage

of allowing for an additional "guard" pixel between the subapertures to reduce the optical crosstalk, while actually reducing the total number of pixels which need to be digitized.

From the above considerations we are left with two options, the Marconi CCD39 and the MIT/LL 64[2]. We recommend the CCD39-based system for the following reasons:

- The convenience of a compact camera head
- Both detector and controller are commercially available components
- Similarity to other Gemini systems and resulting in-house expertise
- The high level of flexibility in the controller to accommodate different readout patterns, etc.
- Lower cost

Detector systems considered

PixelVision ADAPT3

The ADAPT3 is a commercial, off-the-shelf camera system produced by PixelVision, Inc. It consists of a single box enclosing both CCD and controller electronics, and a standard PCI interface card that can be installed in a PC. Five fibre optic cables provide communication between the camera and the interface card. The camera includes a liquid-cooled TEC capable of cooling the detector 45 degrees below ambient temperature. The 80x80 pixel camera can produce frame rates of up to 1500 fps, but the read noise is relatively high. It comes with software and a software developer's kit for 32-bit Windows applications. Unfortunately, when I contacted PixelVision for more information, I was told that they do not produce this camera anymore. They are, however, working on a replacement product for which details are not available yet. They were also uncertain whether a single PC could support 5 separate cameras.

Marconi CCD39

The Marconi CCD39 is the detector used for the Gemini peripheral and on-instrument wavefront sensors. For the purposes of this study, we have also assumed use of a camera head assembly similar to the one used for these WFS systems and an ARC/SDSU2 controller.

The ARC controller is a very flexible and modular system consisting of several circuit boards in a VME-like backplane. It is connected via a fibre optic cable to a VME bus interface card that provides direct memory access to VME memory and a communication link with a VME host. The system is controlled by three DSPs, and is easily programmed to accommodate different applications – essentially everything is under software control, including voltage levels and signal timing. The timing board provides digital timing (or sequencing) signals for controlling the readout of the CCD array and communicates with the VME bus interface card over the fibre optic link. The clock driver board provides up to 24 switched clock voltages to the CCD array, controlled by the timing signals from the timing board. The video processor board amplifies, processes and digitizes the signal from two CCD outputs and provides up to 12 DC bias voltages. The optional utility board provides auxiliary functions, including 11 analog inputs that are multiplexed into an ADC, 4 programmable analog outputs, 16 digital inputs, and 16 digital outputs. It also monitors the power supply voltages and the temperature of the interior of the controller housing. A single backplane can support up to 21 boards in total.

For the CCD39 system, we would need 10 video boards (20 channels), one timing board, and one clock driver board. This results in a total of 12 boards, which conveniently fit in the ARC standard 12-slot backplane. This does not leave room for a utility board, which is normally used for servo control of detector temperature, so temperature control will have to be done by external controllers. There are several manufacturers who make suitable TEC controllers.

For this system we would need an upgraded version of the controller, which can handle a higher data rate and uses a PCI interface card (rather than the VME interface used in the Gemini WFSs). This high-speed version is currently in development – working prototypes of the new timing and PCI interface boards have been built, but production versions are not yet available (projected availability in second quarter 2001). For our purposes, a PMC interface would be more suitable. ARC claims the transition from the PCI to a PMC interface would be a simple matter of form factor, and expects that PMC versions should follow soon.

The Gemini staff has experience with the ARC controllers, as they are being used not only for the A&G WFS systems, but also for the Altair, GMOS, NIFS, and GNIRS instruments. This experience has, however, illuminated some reliability issues with these controllers.

Component / cost breakdown:

ARC 20-channel controller	1 @ $62000	$62000
ARC PCI interface card	1 @ $3000	$3000
TEC packaged CCD39	5 @ $9500	$47500
TEC controller	5 @ $500	$2500
Custom camera housing	5 @ $5400	$27000
Total		**$142000**

Marconi CCD50

The CCD50 is a 128x128 pixel detector originally designed for the ESO VLT NAOS system. It is available from Marconi by special order. For our comparisons, we have assumed the use of a high-speed ARC/SDSU2 controller, as for the Marconi CCD39, although in this case we would only be running one CCD. We would need only 8 video boards, leaving room in a 12-slot backplane for a utility board, which could handle the temperature control function. We have not been able to get any detailed information on the CCD50 device, although the characteristics would probably be similar to other standard Marconi detectors, such as the CCD39.

Unfortunately, due to the odd spacing of the quad cells (three pixel pitch) and the architecture of the device, every pixel must be digitized. The controller cannot skip over the guard pixels because they will occur at different points for each output. A timing analysis showed that the ARC controller is not quite fast enough to achieve the required read out time of 1 ms. The speed of the controller is limited by the 1 us conversion time of the 16-bit ADCs and the 12.5 Mpixel/s transmission rate of the fibre optic transmitter.

Component / cost breakdown:

ARC 16-channel controller	1 @ $52000	$52000
ARC PCI interface card	1 @ $3000	$3000
TEC packaged CCD50	1 @ ?	?
TEC power supply	1 @ $300	$300
Custom camera housing	1 @ $5400	$5400
Total		**$60700+CCD**

Marconi CCD60

The CCD60 is a new product, launched in August 2000 with projected availability sometime in 2001. It makes use of Marconi's new L3CCD (Low Light Level CCD) technology, which involves an avalanche process to enhance the signal. This enables the device to achieve very low equivalent read noise levels, but introduces extra shot noise. According to approximate models provided by EEV, the flux level at which the increased shot noise dominates over the reduced read noise is about 75 detected photons. We estimate that the laser guide star signal levels will be around 200-400 detected photons. In a photon-noise dominated application such as this, the L3CCD technology is of no advantage.

The CCD60 is a 128x128 pixel frame transfer device with a single output. It comes integrated with the drive electronics which are capable of delivering 12-bit data at 16 MHz pixel rates (~1 kHz frame rate) over a parallel interface. Initial devices are front-side illuminated with a peak QE of 35%, but thinned back-side devices are under development. Pricing for this system is not available yet.

MIT/LL 128

The 128x128 pixel camera developed by Lincoln Labs has 16 signal channels. There are eight outputs along both the top and bottom of the detector. These outputs are directed through 16 analog signal chains with amplifiers and correlated-double samplers and the resulting signal is transmitted (up to 3m) to four digitizer boards, each with four 14-bit analog-to-digital converters (ADC). The ADCs pass their data on to the host computer over an arrangement of parallel RS422 cables to DMA interfaces in the host. The standard configuration is to have each digitizer board multiplex its four channels into one 16-bit parallel stream and then combine two of these streams into each of two 32-bit parallel cables. This configuration requires two 32-bit DMA interfaces in the host computer. The current reconstructor configuration favours a single 32-bit stream that would be fed to the parallel I/O ports of the processor boards.

The readout sequence is directed by a timing/control board. The CCD clock waveforms are generated by pre-programmed PLAs, so the readout configuration is essentially fixed. However, it is possible to program more than one set of clock waveforms into the PLAs and switch between them.

Component / cost breakdown:

LL128 CCD and controller	1 @ $200000	$200000
32-bit VME/PCI interface card	2 @ $2000	$4000
Total		**$204000**

MIT/LL 64

This is a 64x64 pixel, four output version of the above camera. We would need five CCDs and therefore twenty signal channels. The system would consist of five sensor boards, each with a single CCD and four analog channels, five four-channel digitizer boards, and one control/timing board.

Component / cost breakdown:

5 LL64 CCDs and controller	1 @ $270000	$270000
32-bit VME/PCI interface card	2.5 @ $2000	$5000
Total		**$275000**

An alternative option would be to purchase only the TEC-packaged CCDs, and run them with an ARC controller as in the CCD39 option. There is no significant technical advantage to this option. The one difference is that the CCD array is smaller, so a small amount of time could be saved in flushing out undigitized peripheral pixels.

Timing and noise calculations

In order to check the feasibility of reading the detectors under consideration within the timing constraints, we created a spreadsheet to calculate the readout rate as well as the corresponding noise factors. The spreadsheet consists of two worksheets. The first sheet, labelled “Overview” contains calculations of the raster geometry, exposure time, signal strength, and the various noise contributions to arrive at a signal-to-noise ratio (SNR). The second sheet, labelled “CCD timing” has a detailed calculation of the readout timing of each detector. For those options using an ARC controller, the timing is broken down into considerable detail because of our intimate knowledge of the operation of this controller. There is a column for each of the detector options described above, including the option of using a LL64 detector with an ARC controller.

On the “Overview” sheet, the first section describes the optical configuration including the pixel size, the array size, the pitch of the Shack-Hartmann lenslet array, and the focal reduction from the Shack-Hartman focal plane to the detector plane. This section determines how the Shack-Hartman array maps to the various detector geometries. The second section summarizes the readout timing, which is calculated in detail on the “CCD timing” sheet. The third section contains a rough estimate of the signal strength based on the projected flux of the laser beacon, the estimated throughput of the optics, the quantum efficiency (QE) of the detector, and the exposure time. The QE shown for the CCD60 device assumes that backside-illuminated versions will be available. The fourth section outlines the various noise contributions, including

the read noise (based on calculations from the “CCD timing” sheet), the dark current, the sky background, and the shot noise from the signal itself. The total noise is a quadrature sum of the different noise sources. For the CCD60, the effect of the avalanche gain is taken into account, which effectively doubles the shot noise. The gain is estimated based on the limited information available for this device. The last line shows the signal-to-noise ratio based on the calculated signal strength and the total noise.

On the “CCD timing” sheet, the first section describes the architecture of the detectors, including the number of rows and columns, the number of underscan pixels, and the number of outputs. This section also has the number of subapertures, the number of digitised pixels per subaperture, the number of undigitized (guard) pixels per subaperture, and the offset to the subaperture closest to the output. The LL64, CCD50and LL128 show only one subaperture equal to the entire array because for these architectures, the entire array must be digitised.

The second section of the “CCD Timing” sheet lists the timing parameters related to the waveform sequencer DSP of the ARC controller. The third section lists some timing parameters taken from the CCD data sheets, and some numbers derived from these parameters. One of the most important parameters is the dual slope integration time. This number describes how much time is spent integrating the video signal from each pixel before it is sampled, and is directly related to the read noise. The number shown is the sum of the reset level and signal integrations. This number has been maximized under the constraints of the total frame time to get the lowest read noise.

The third section of the “CCD Timing” sheet is the detailed breakdown of the readout timing, ordered in the same way the readout is actually performed. The last line is the time required to flush the last pixels from the analog-to-digital converter (ADC). Because the ADC is pipelined, an extra two digitization cycles are required. The total frame time, in bold, is a sum of the individual times from this section.

The fourth section shows the maximum readout time allowed, based on the desired wavefront sampling rate and latency requirements and the resulting maximum dual slope integration time. This section also calculates the total instantaneous pixel rate, for data transport and processing considerations. It can be seen from this that for the CCD50, the pixel rate exceeds the maximum transmission rate of the fibre optic tranceiver of the ARC controller.

The last section of the “CCD Timing” sheet has a calculation of the read noise based on the output amplifier characteristics, the dual slope integration time and the noise added by the signal processing chain. For the LL64 and LL128, the details of the amplifier and signal chain are unknown, so the noise estimates from the manufacturer are inserted. Characteristics of the CCD60 amplifier and the corresponding integration time were estimated from available information.

Table 1: Signal-to-Noise Ratio Overview

MCAO LGS WFS CCD configuration
(shaded cells are inputs, the rest are calculated values)

24-Mar-01

Considerations for Raster Geometry	Comments	CCD39	LL 64	LL 64 (ARC)	CCD50	LL128
Pixel size (um)		24	21	21	24	21
Array size (pixels)		80	64	64	128	128
Array size (mm)		1.92	1.344	1.344	3.072	2.688
SH lenslet pitch (mm)		0.5	0.5	0.5	0.5	0.5
SH lenslet array size (# lenslets)		16	16	16	16	16
SH lenslet array size (mm)		8	8	8	8	8
Lenslet arrays per detector		1	1	1	5	5
SH focal plane to detector plane focal reduction		5.208	5.952	5.952	6.945	7.936
Lenslet pitch at detector plane (um)		96.0	84.0	84.0	72.0	63.0
Lenslet pitch at detector plane (pixels)		4.00	4.00	4.00	3.00	3.00

CCD Readout Timing (for 1 kHz Sampling Rate)		CCD39	LL 64	LL 64 (ARC)	CCD50	LL128
Frame rate (Hz)		800	800	800	800	800
Allowed frame time (ms)		1.00	1.00	1.00	1.00	1.00
Frame Transfer Time (ms)		0.03	0.03	0.05	0.05	0.05
Total frame time (ms)		1.00	1.00	0.99	1.12	1.00
Exposure Time (ms)	Frame rate - Frame Transfer Time	1.22	1.22	1.20	1.20	1.20

Signal Quality		CCD39	LL 64	LL 64 (ARC)	CCD50	LL128
Total LGS flux from 500-900 nm (ph/s/cm^2)		2.50E+02	2.50E+02	2.50E+02	2.50E+02	2.50E+02
Average Transmittance of the Atmosphere from 500-900 nm		0.88	0.88	0.88	0.88	0.88
PM Collecting Area (cm^2)		503990.0015	503990.0015	503990.0015	503990.0015	503990.0015
Reflectance of mirror		0.962	0.962	0.962	0.962	0.962
Number of mirrors		8	8	8	8	8
Science beamsplitter transmittance		0.993	0.993	0.993	0.993	0.993
NGS/LGS beamsplitter transmittance		0.99	0.99	0.99	0.99	0.99
Air-glass interface transmittance		0.998	0.998	0.998	0.998	0.998
Number of air-glass interfaces		30	30	30	30	30
Fraction of Light per Sub-aperture		0.00390625	0.00390625	0.00390625	0.00390625	0.00390625
Average QE of CCD from 500-900 nm(e-/ph)		0.85	0.85	0.85	0.85	0.85
Integration Time (s)		0.001220	0.001220	0.001201	0.001201	0.001200
Signal on the detector (e-/subaperture)		304.89	304.99	300.33	300.33	299.99

Noise contributions		CCD39	LL 64	LL 64 (ARC)	CCD50	LL128
CCD Read Noise (e-)		5.05	5.00	5.02	too fast (FO)	5.00
Dark current (room temp) (e-/px/s)		7.50E+04	2.76E+04	2.76E+04	1.00E+04	2.76E+04
CCD Temperature (Celsius)		-40	-40	-40	-40	-40
Dark current (e-/px/s)		136.26	50.14	50.14	18.17	50.14
Dark Noise (e-/px)		0.41	0.25	0.25	0.15	0.25
Plate scale (px/arcsec)		1.00	1.00	1.00	1.00	1.00
Flux for a 0th Magnitude Star (ph/s/cm^2/nm) @550nm		9.79E+03	9789	9789	9789	9789
Sky background (ph/px/s/cm^2)	20th magnitude per arcsec^2, 400nm bandwidth	3.92E-02	3.92E-02	3.92E-02	3.92E-02	3.92E-02
Sky background (e-/px/s)		39.15	39.15	39.15	39.15	39.15
Sky background noise (e-/px)		0.22	0.22	0.22	0.22	0.22
Photon noise from signal (e-/px)		8.73	8.73	8.67	8.67	8.66
Gain	CCD60 only					
Total noise (e-/subaperture)	Includes gain effects for CCD60	20.19	20.14	20.04	#VALUE!	20.01
SNR		15.1	15.1	15.0	#VALUE!	15.0

Table 2: Timing Model

MCAO LGS WFS CCD timing model
24-Mar-01

	CCD39	LL 64	LL 64 (ARC)	CCD50	LL128	CCD60
Number of CCDs	5	5	5	1	1	1
Rows (active area)	80	64	64	128	128	128
Rows (storage region)	80	64	64	128	128	128
Rows (dark reference)	0	0	0	0	0	0
Columns (active area)	80	64	64	128	128	128
Columns (dark reference, per port)	0	0	0	0	0	0
Underscan pixels	4	4	4	4	4	271
Ports (per row)	2	4	4	8	16	1
Ports (per column)	2	1	1	2	1	1
Sub apertures (n x n)	16	1	16	1	1	42
Digitized pixels/aperture (n x n)	2	64	2	128	128	2
Undigitized pixels/aperture (each dimension)	2	0	2	0	0	1
X position of subaperture (unbinned)	8	0	0	0	0	2
Y position of subaperture (unbinned)	8	0	0	0	0	2
ARC/SDSU2 controller DSP parameters						
Parallel delay (wave table step size, or clock overlap)	1.00E-07		1.00E-07	1.00E-07		
Serial delay (wave table step size, or clock overlap)	4.00E-08		4.00E-08	4.00E-08		
DSP instruction time	4.00E-08		4.00E-08	4.00E-08		
Loop overhead	1.60E-07		1.60E-07	1.60E-07		
Timing parameters						
Parallel to serial delay time	2.00E-06		2.00E-06	2.00E-06		
Serial to parallel delay time	1.00E-06		1.00E-06	1.00E-06		
Dual slope integration time (2T)	2.16E-06		2.20E-06	4.00E-07		1.13E-07
Parallel transfer time	7.60E-07		7.60E-07	7.60E-07		
Serial transfer time (one pixel, flushing)	2.80E-07		2.80E-07	2.80E-07		
Serial transfer time (one pixel, binning)	2.40E-07		2.40E-07	2.40E-07		
Serial register flush	1.18E-05		4.76E-06	4.62E-06		
Frame timing						
Frame transfer	3.04E-05	3.00E-05	4.86E-05	4.86E-05	5.00E-05	5.00E-05
Flush initial unread rows (YSTART)	1.78E-05		4.76E-06	4.62E-06		
Delay before serial clocking	2.00E-06		2.00E-06	2.00E-06		
Flush unread pixels (XSTART)	3.72E-06		1.48E-06	1.48E-06		
Serial transfer	2.40E-07		2.40E-07	2.40E-07		
Dual slope integration	2.16E-06		2.20E-06	4.00E-07		
Pixel overhead	4.00E-07		4.00E-07	4.00E-07		
Total time (one pixel)	2.80E-06		2.84E-06	1.04E-06		
Skip guard pixels	4.80E-07		4.80E-07	0.00E+00		
Total time (one subraster row)	6.08E-06		6.16E-06	1.33E-04		
Flush remaining pixels in the row	0.00E+00		0.00E+00			
Total time (one full row)	4.86E-05		2.46E-05	1.66E-05		
Total time for one row of subrasters	9.73E-05		4.93E-05	2.13E-03		
Flush rows between subrasters	2.35E-05		9.52E-06	0.00E+00		
Total time for all subrasters	9.43E-04		9.31E-04	1.06E-03		
Flush ADC pipeline	6.64E-06		6.64E-06	6.64E-06		
Total frame time	**9.98E-04**	**1.00E-03**	**9.91E-04**	**1.12E-03**	**1.00E-03**	**1.00E-03**
Maximum frame read time	1.00E-03	1.00E-03	1.00E-03	1.00E-03	1.00E-03	1.00E-03
Total number of digitised pixels per port	2.56E+02	1.02E+03	2.56E+02	1.02E+03	1.02E+03	7.06E+03
Maximum dual slope integration time (2T)	2.17E-06		2.23E-06	2.78E-07		
Instantaneous pixel rate (all ports, all CCDs)	7.14E+06	2.05E+07	7.04E+06	1.54E+07	1.64E+07	7.06E+06
Maximum pixel rate (fibre optic tranceiver limit)	1.25E+07		1.25E+07	1.25E+07		
Read noise						
Responsivity (µv/e-)	4.50		4.50	5.00		1.30
1/f corner frequency	1.50E+05		1.50E+05	1.50E+05		1.50E+05
Output circuit noise (e-/px)	4.86		4.83	9.59		34.59
Controller noise (e-/px)	1.38		1.37	2.69		9.72
Total read noise (e-/px)	**5.05**	**5.00**	**5.02**	**too fast (FO)**	**5.00**	**35.93**